ATTACHMENT AC

EXHIBIT 15

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Thread: BFL ASIC Status

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02-25-2013, 09:54 PM #11

BFL_Josh

Employee

Blog Entries: 2
Mentioned: 151 Post(s)
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Latest Blog: Busy day!

25 Feb 2013 Update

I know people have been waiting on an update for awhile. The simple fact of the matter is there hasn't been any solid updates to offer. I know people are desperate and starving for information and I wish I could provide new information every day, but some days there just isn't new information. Luckily there is some new information today. It's not the best information (such as we are shipping today!) but it is at least an update.

We had expected the bumping to be done by now, as per the previous update(s). That has not been completed yet. There are a number of reasons why this is the case, and we are not pleased with any of them. The bumping facility, which we have no direct contact with, did not complete the NRE on the timeline we had spoke to the

Latest Thread: Duplicate IP Report for 04-26-2014

Join Date: Aug 2012
Posts: 2,153
Blog Entries: 2

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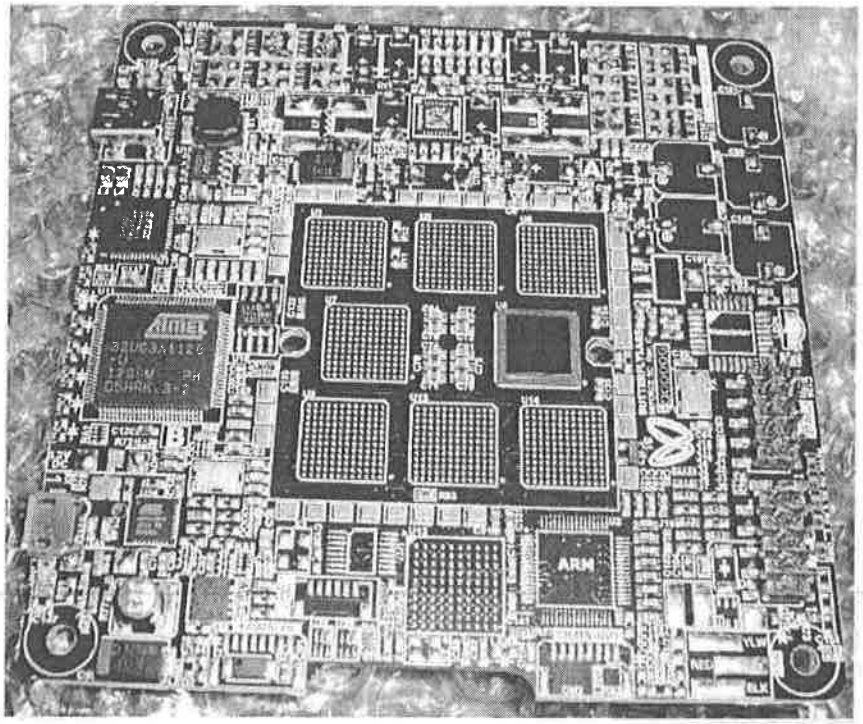
packaging facility about. As I've written in previous posts, we are dealing with such an accelerated time scale that all of these facilities simply aren't used to dealing with. It's been a learning experience for both us and for the facilities we are using. The upside, such as it is, is that going forward, we will have all the large, time sucking hurdles already out of the way and the rest of the chips should breeze through without issue, as all the NRE, tooling, design, planning and machines will already be configured for what we need.

Since Friday we have been, in a word, agonizing over how to make up for lost time. Obviously, we can't make up for all the lost time, but what we have decided is to effectively burn (this is not a technical term, I simply mean we are using one of the wafers for testing instead of creating chips out of it) one of the initial six wafers for testing. This is definitely not something we wanted to do, as it will reduce our initial chip count from a potential 6000 to 5000 chips for the first set of wafers. We are doing this because it will buy us 7 - 12 days for the second set of wafers (and the remaining set of wafers down the road). The time frame between the 1st set of wafers and the 2nd set of wafers should be reduced to a matter of a few days.

Why are we burning the wafer, what advantage does that give us and how can that accelerate the timeline? As many of you already know, we have had the 2nd set of wafers holding with the last layers being unfinished until we confirm we have everything the way we want it on the first set of wafers. We've already started the process to continue laying down layers up until about the last 5 layers or so - by burning one of our precious wafers, we can send it to the ASIC engineers who can essentially wire bond it manually and test the chips, but the wafer will become useless for creating usable chips. By doing this, they will verify that everything is how it needs to be and we can give the foundry the go-ahead to finish the second set as well as the bulk of the chips immediately. The second set of wafers should be done and on their way to us by the time we get chips in house in KC, and the bulk wafers should be done shortly after that.

The test wafer is already on it's way to the ASIC labs and should arrive tomorrow. Presumably it will take a better part of the day to get everything situated and for the testing to begin, so I don't expect to hear anything until late Tuesday or sometime on Wednesday assuming everything goes well. In the meantime, the bumping facility will be bumping the remaining 5 wafers, which should be shipping out on Friday to the packaging house, whom we are paying extra to stay on for the weekend and start the packaging process. We expect at least some of the chips to be on their way to Chicago by Tuesday, where they will be mounted and sent out to our engineers and KC for testing and final MCU programming. At that point, once the MCU programming is confirmed we'll begin assembling the units. Right now, I'm planning on a week from Friday to be the day, but I'm just gonna say that's subject to change at the moment, although I don't anticipate a change right now.

The ASIC team has promised me pictures of the wafer tomorrow, Tuesday the 26th. As soon as I get those, I will be posting them. As soon as I hear something with regards to the chip testing, I will be posting that as well. If I'm not posting an update, it's because there's nothing new to report.



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03-15-2013, 10:57 PM #19

BFL_Josh

Employee

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Mentioned: 151 Post(s)
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Latest Blog: Busy day!
Latest Thread: Duplicate IP Report for 04-26-2014

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15 March 2013 Update

It's been a long couple days here at the labs! Trying to test the chip in the test rig has been exceptionally trying and it turns out it's due to a bad socket on the tester. Initially we were concerned there might be a problem with the bumping or substrate, but fortunately we had tested the chips prior with the wire bonding technique, so we knew they worked. Getting the test boards made proved to be fortuitous as well, since we were able to bypass the test rig completely and bring the chips up on the board. By doing so, we were able to finally identify that the problem was related directly to the test rig and not any intermediate process or step.

Bringing a chip to life in situ on a board is not the easiest thing, so it has been slow going. The chip was responding properly on the board late this afternoon and we will be picking up the process in the morning. We hope to have a more complete test by Saturday night or Sunday sometime. Meanwhile, we will also be hard soldering a chip into place for use in the test rig and replacing the socket to allow the bulk testing to finish. In some other positive news, we've not found a single bad chip yet, which could mean our yield rate will be exceptionally high... maybe we just got lucky out of the 50 chips we have available on boards so far, but it seems unlikely. So that may mean the vast majority of our chips will be usable.